

FIG. 1. Event timing adjustment device.

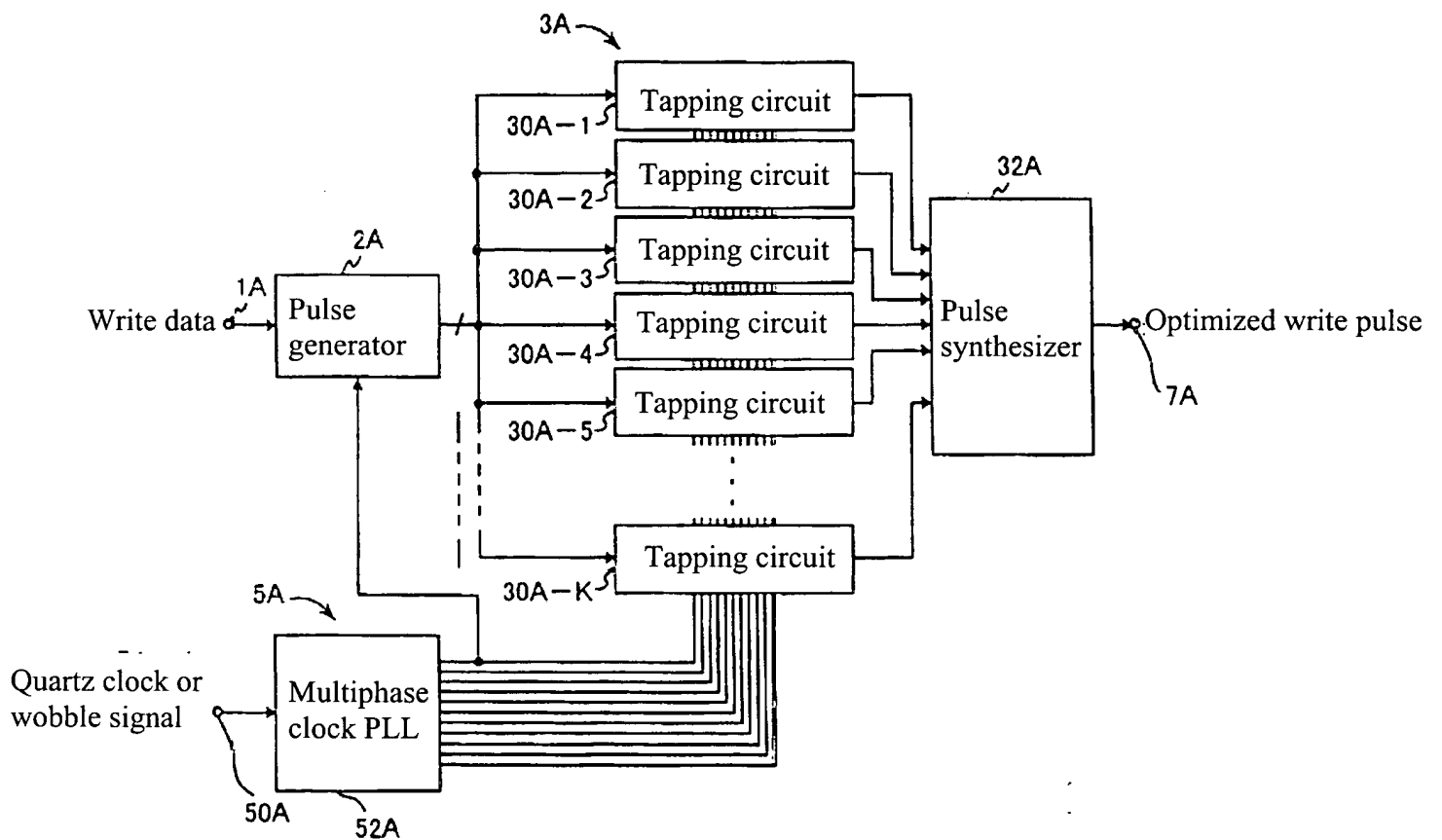


FIG. 2. Pulse width adjusting device A.

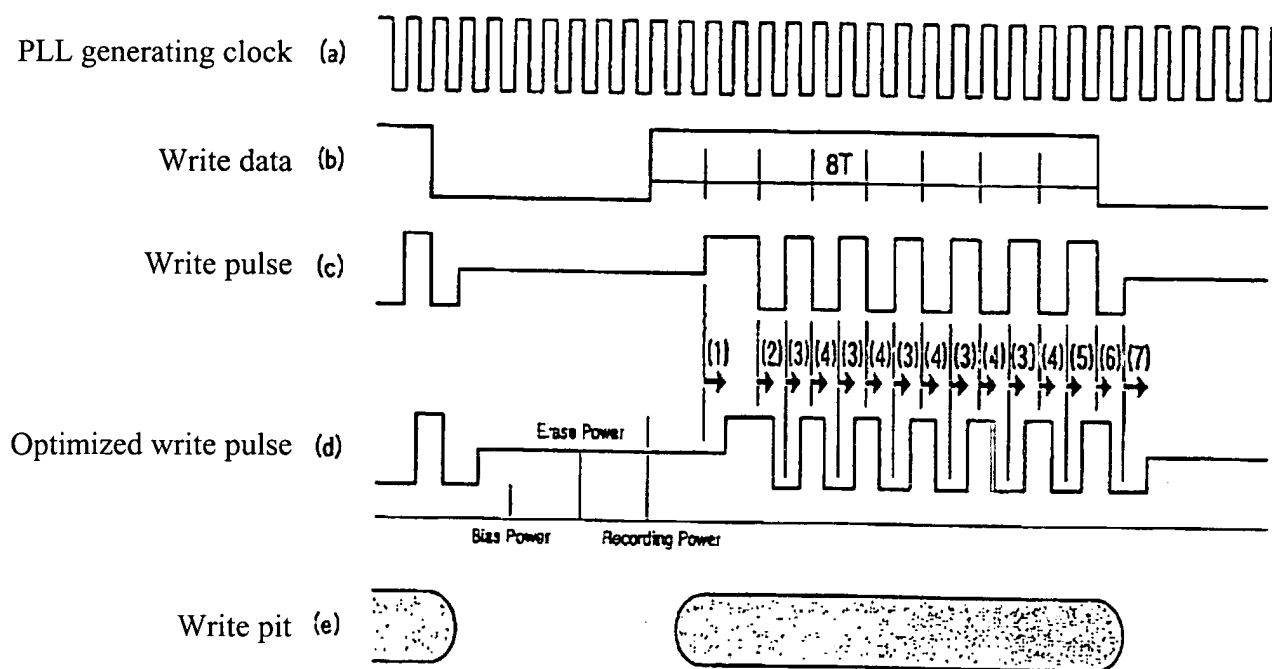


FIG. 3

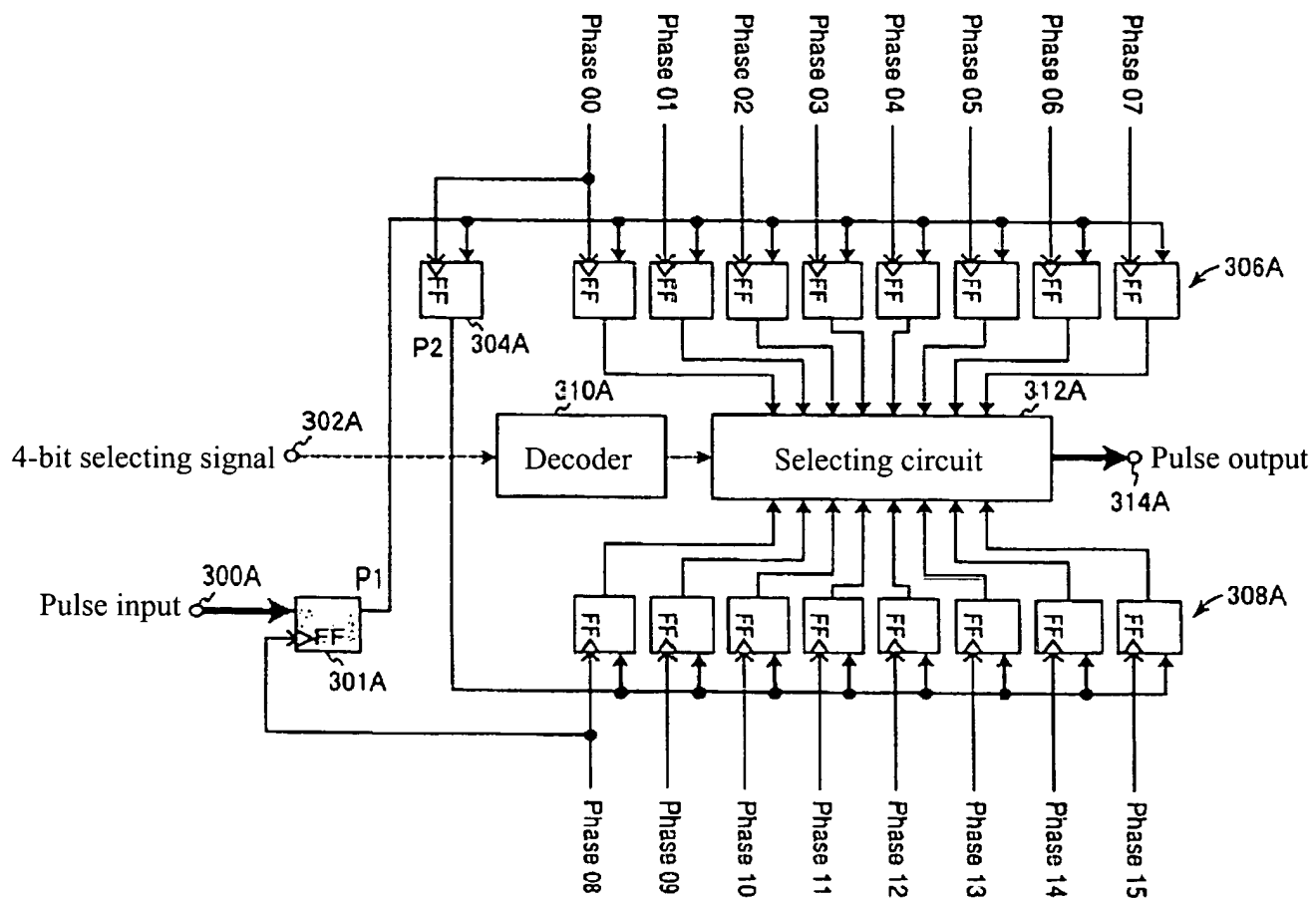


FIG. 4. Delay tapping circuit 30A-k

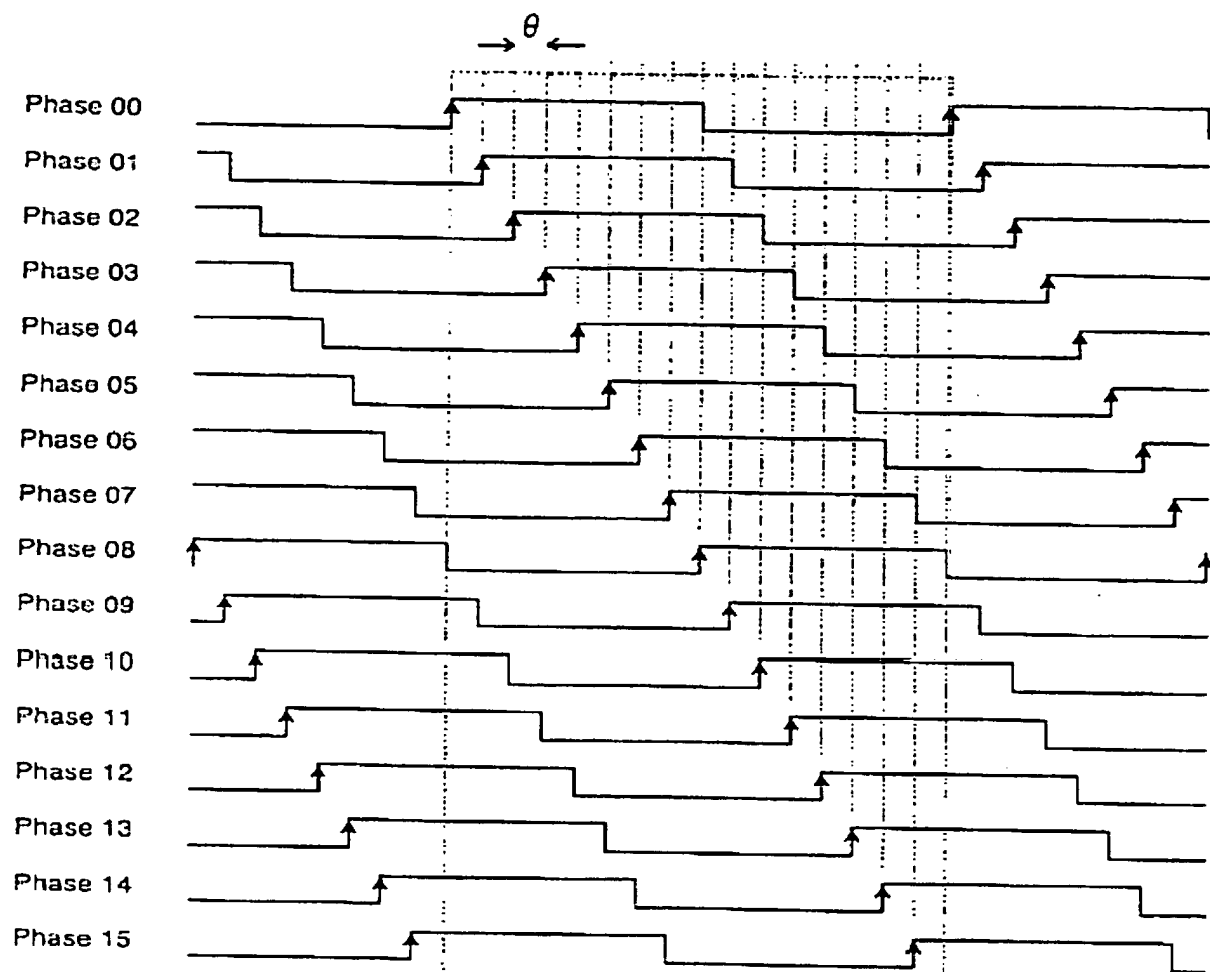


FIG. 5

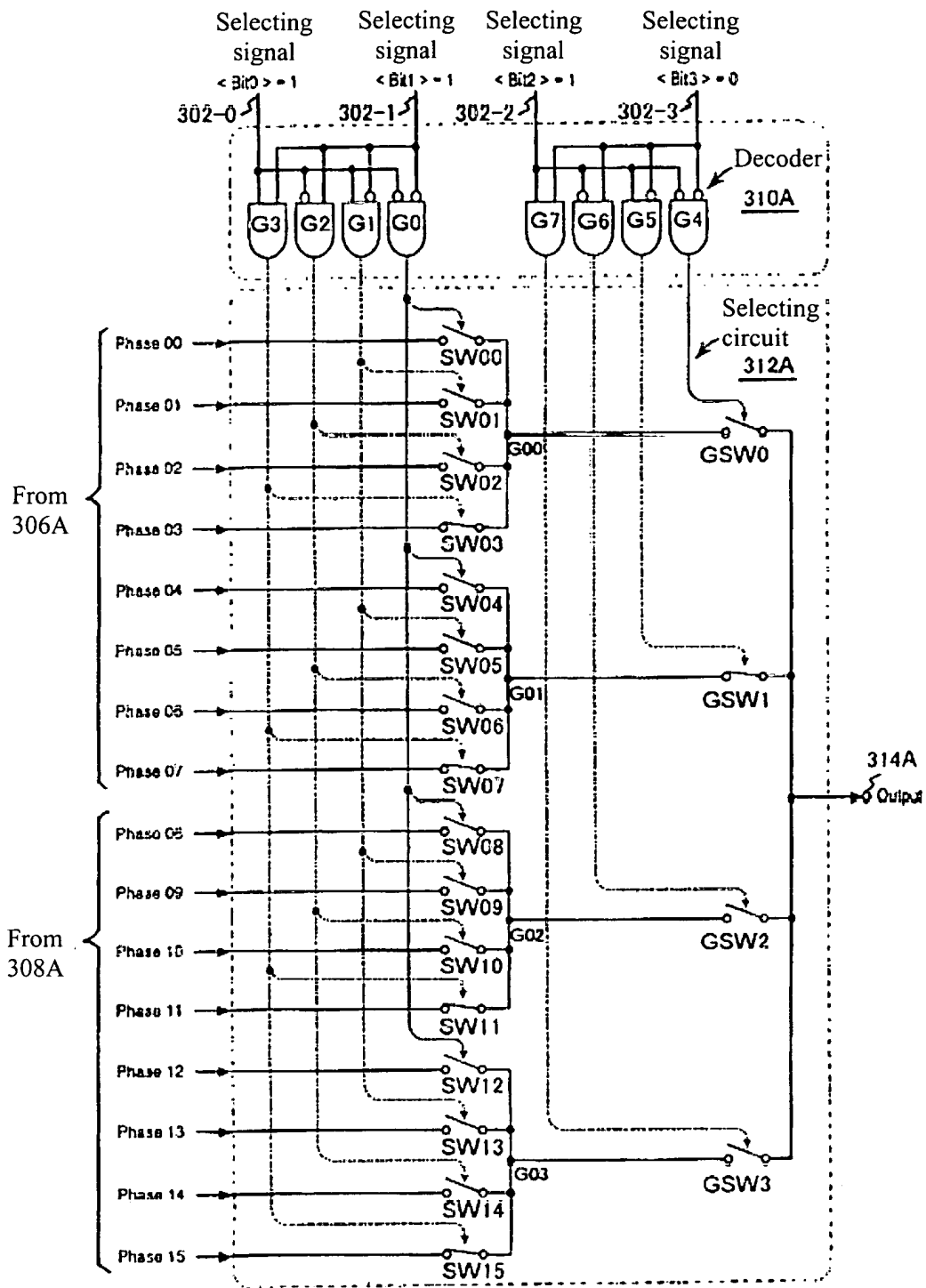


FIG. 6

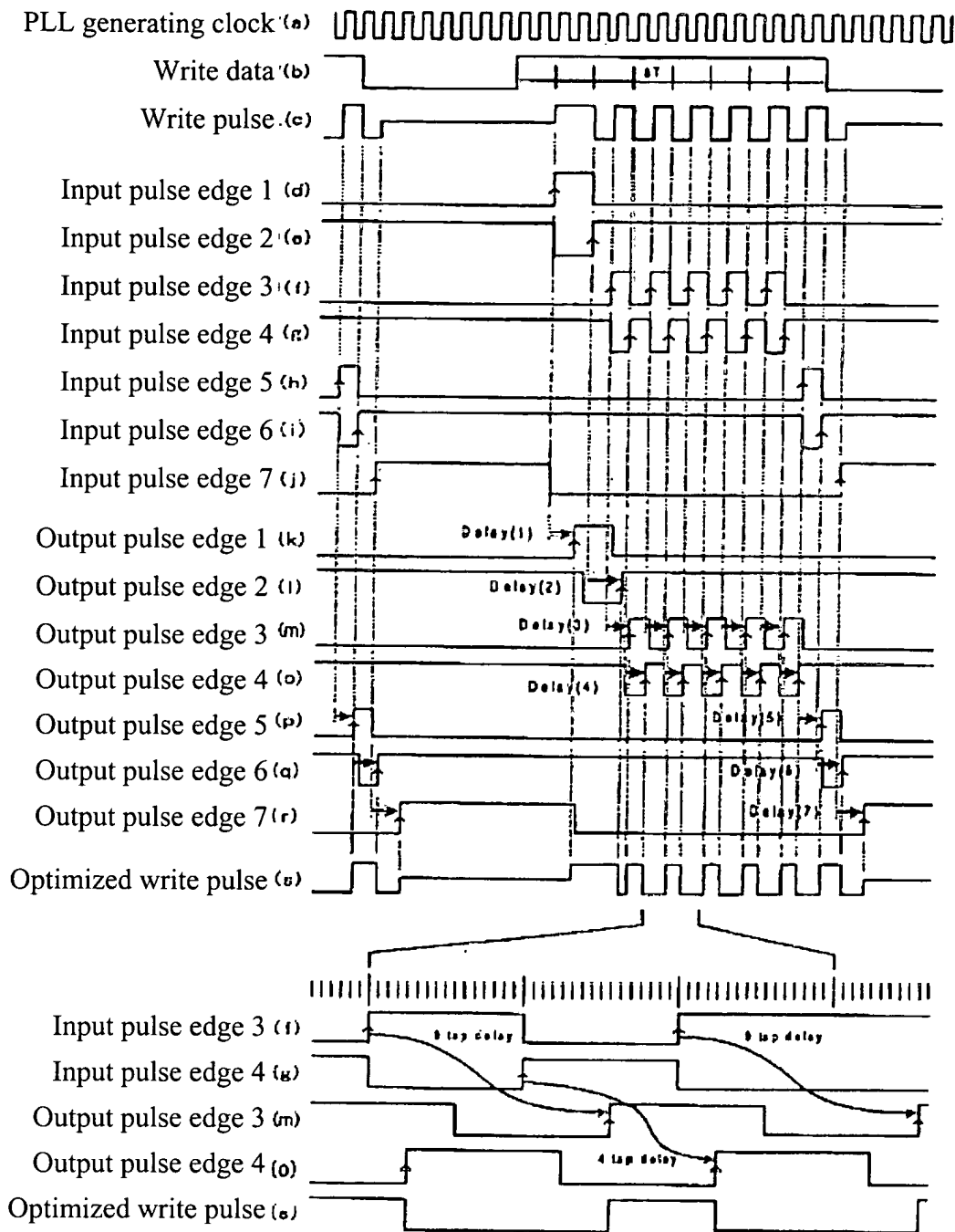


FIG. 7

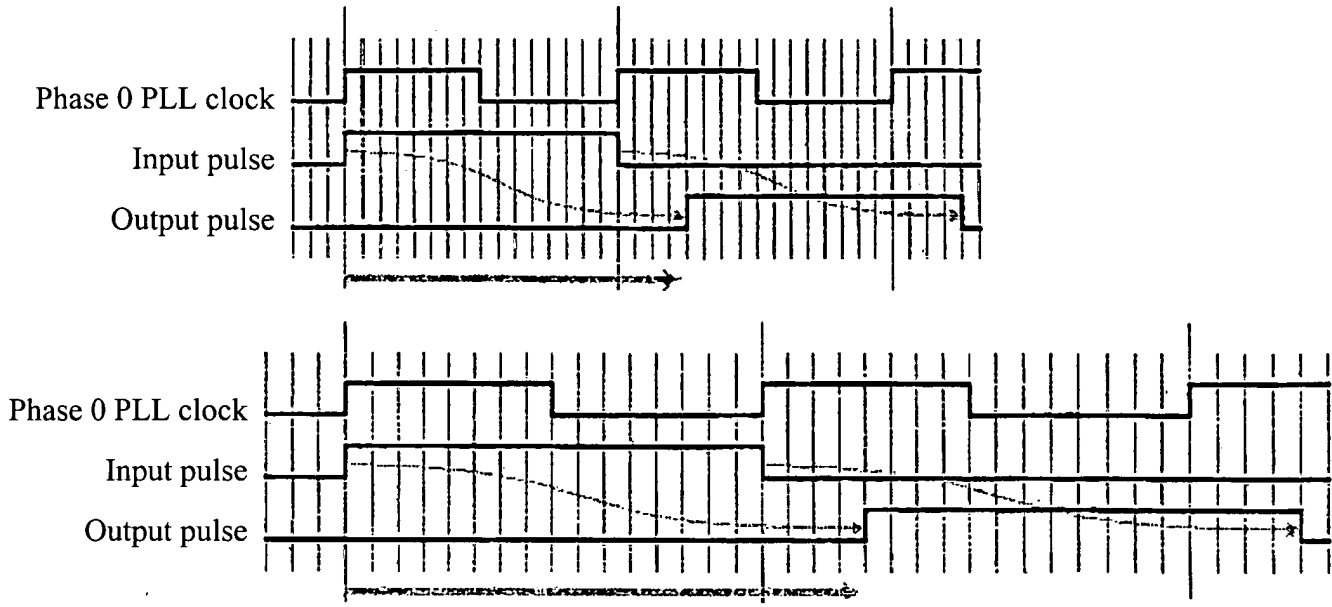


FIG. 8

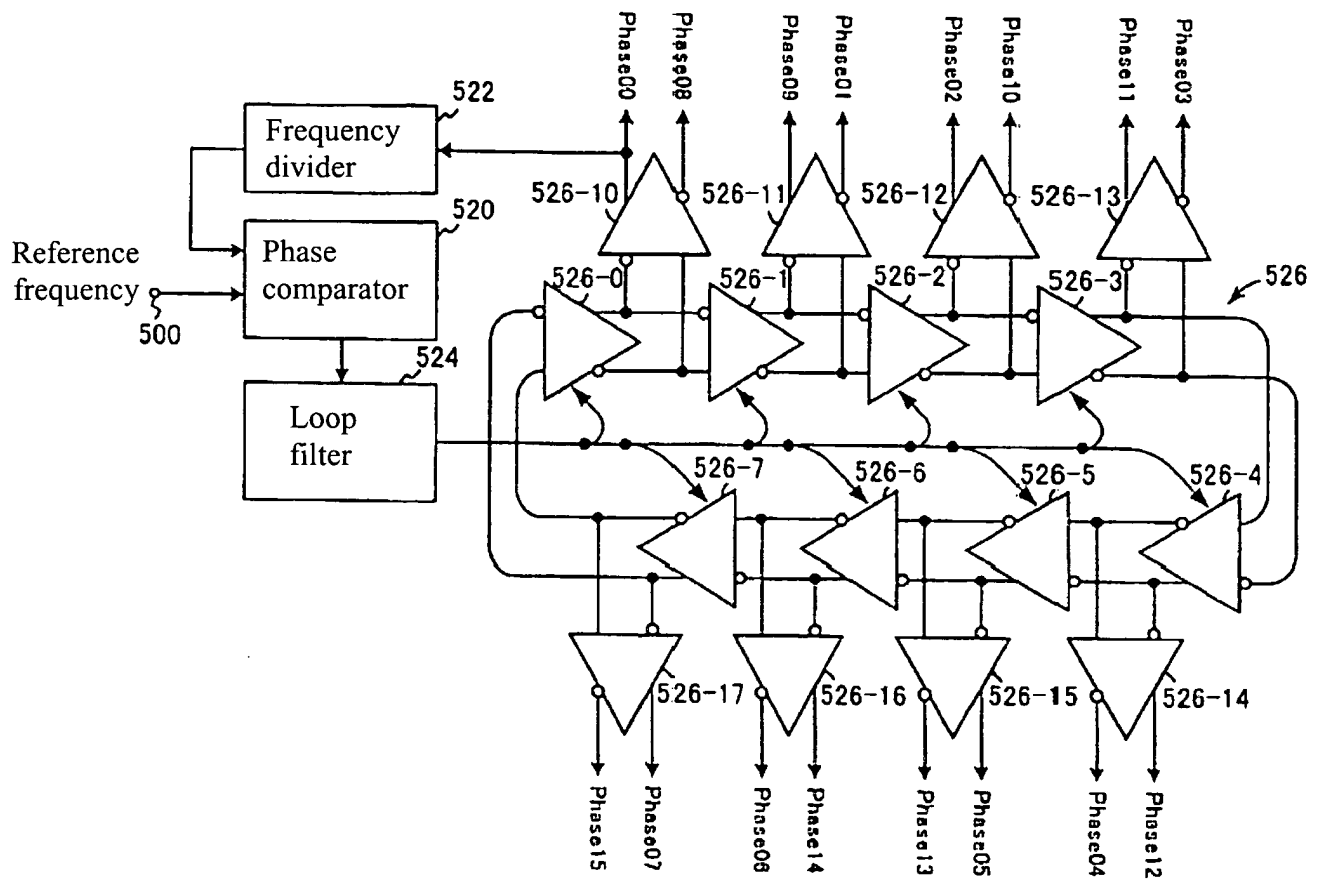


FIG. 9. Multiphase clock PLL circuit 52A.



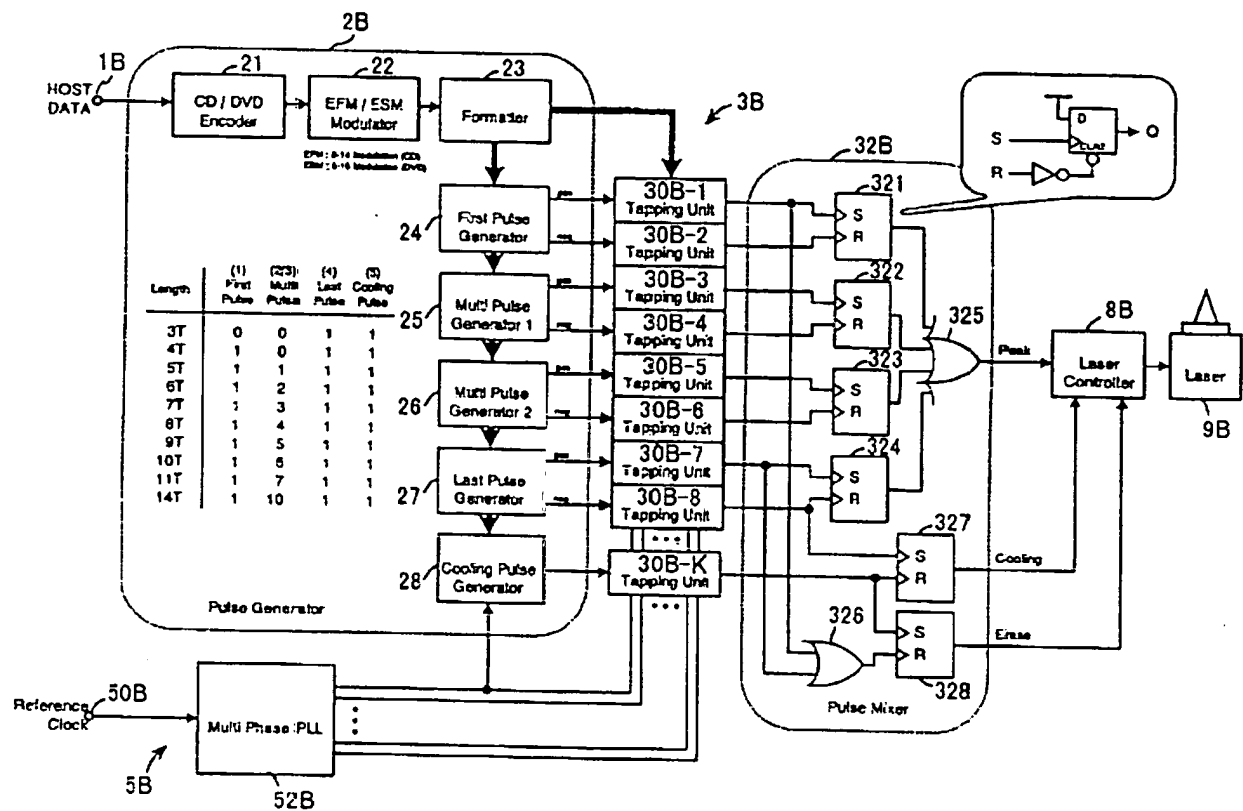


FIG. 10. Optical disk recorder B

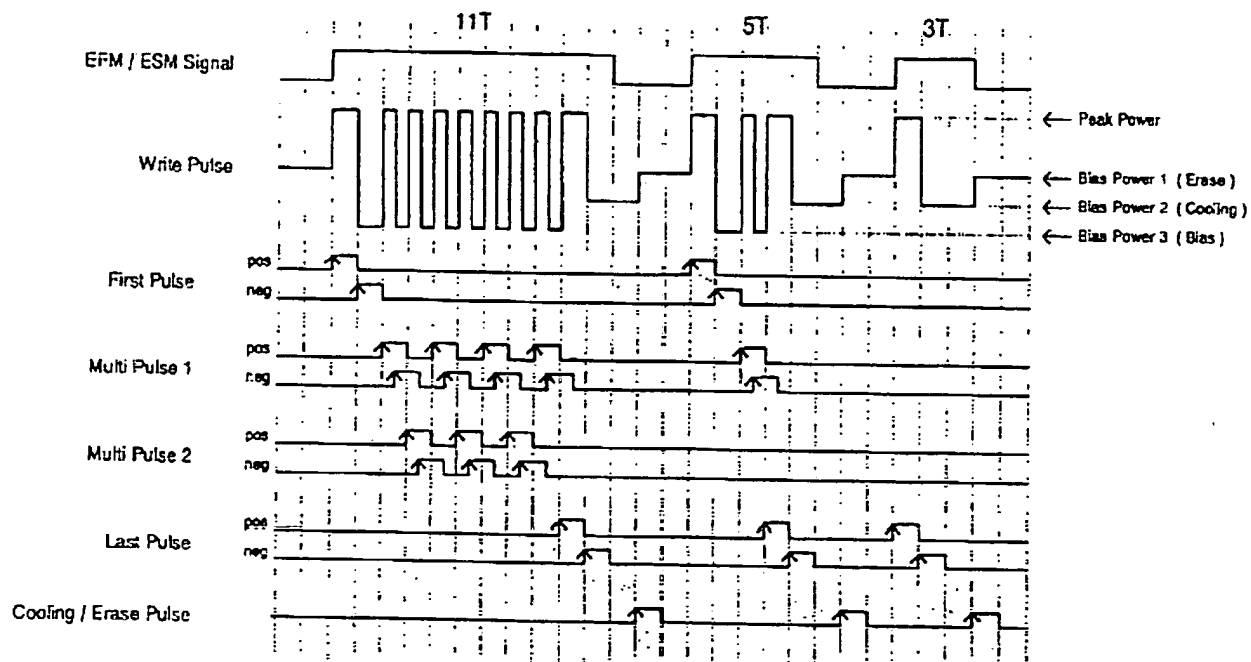


FIG. 11

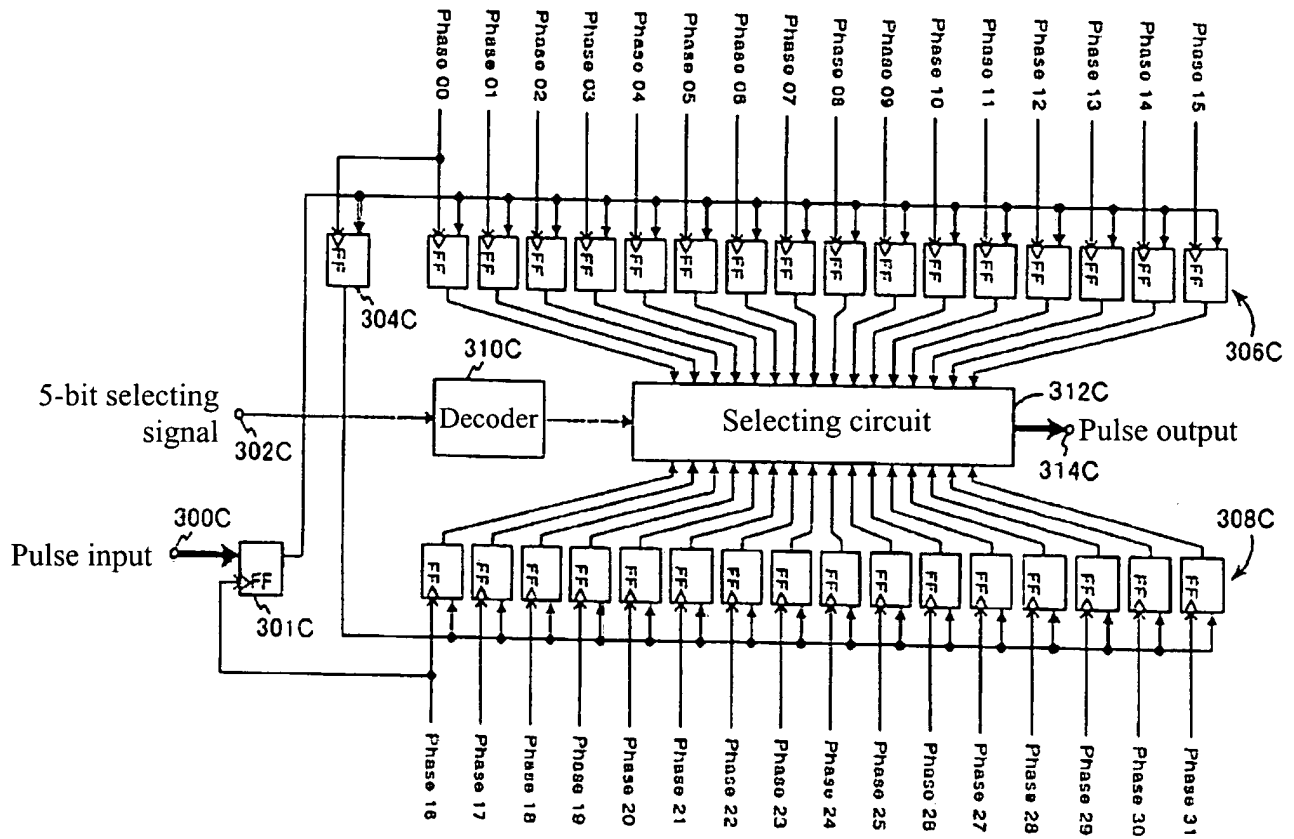


FIG. 12. Delay tapping circuit 30C

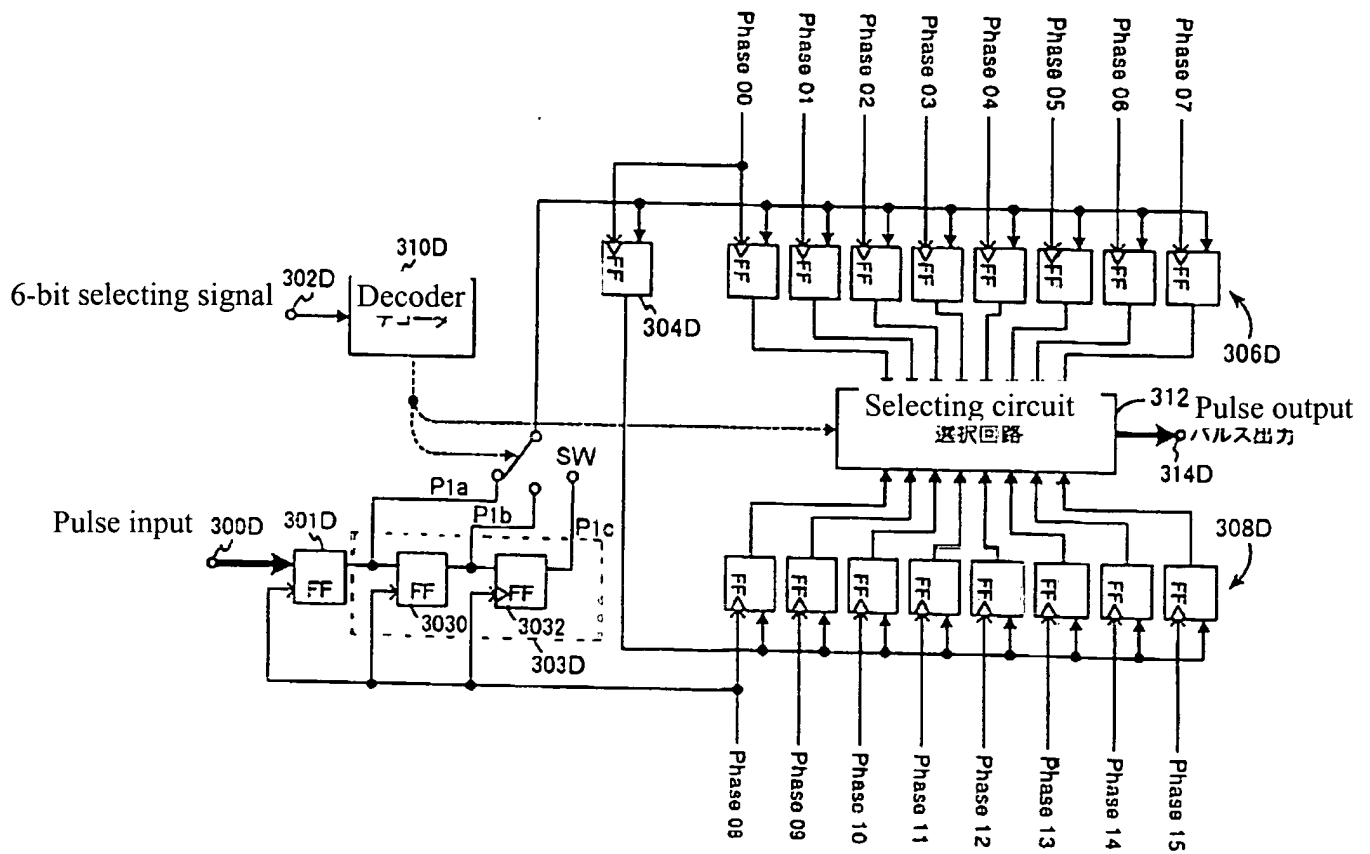


FIG. 13. Delay tapping circuit 30D

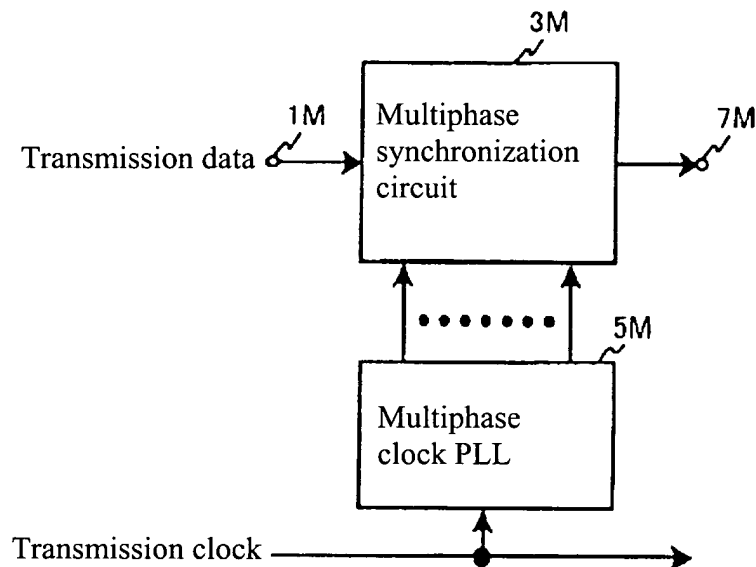
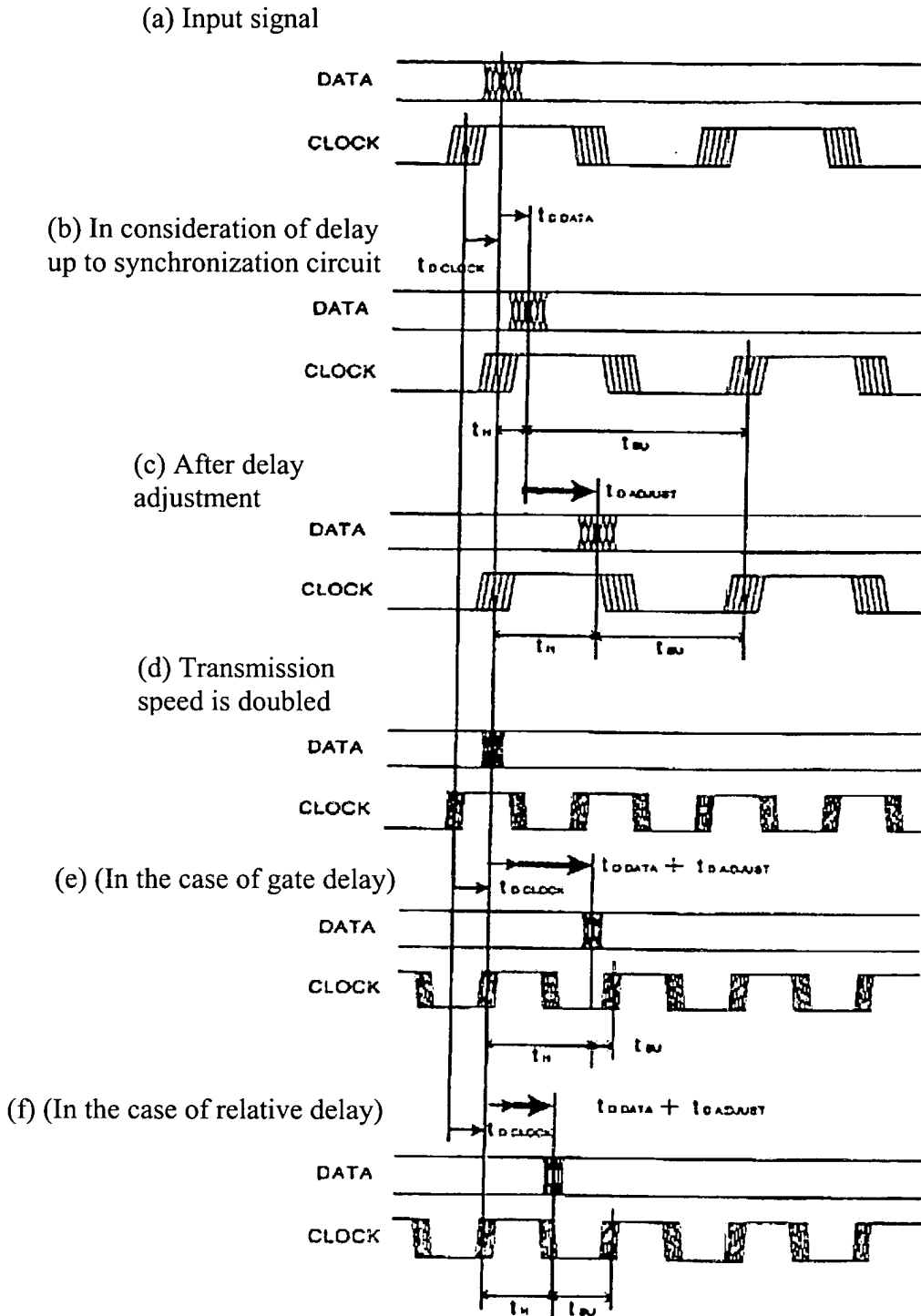


FIG. 14. Synchronization device M.



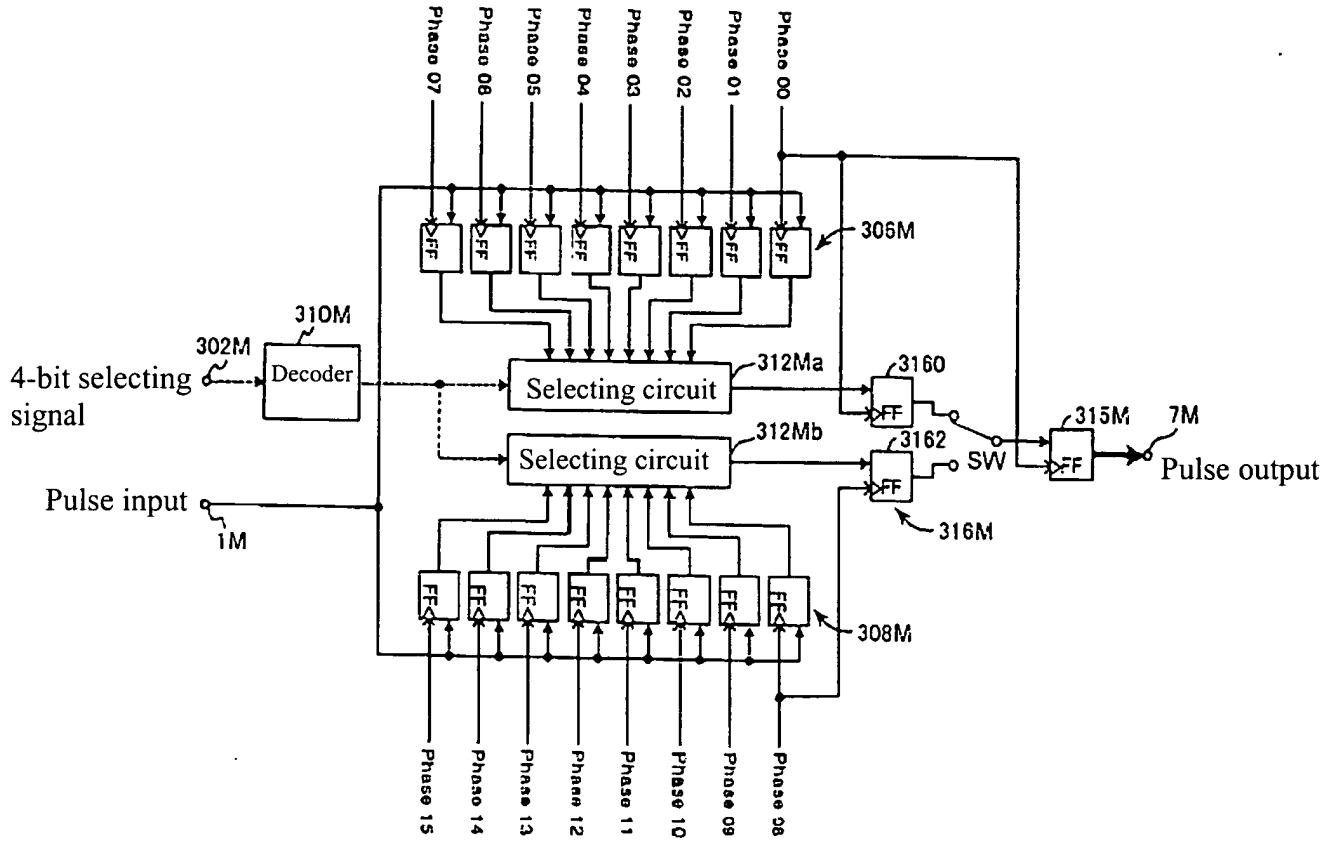


FIG. 16. Multiphase synchronization circuit 3M

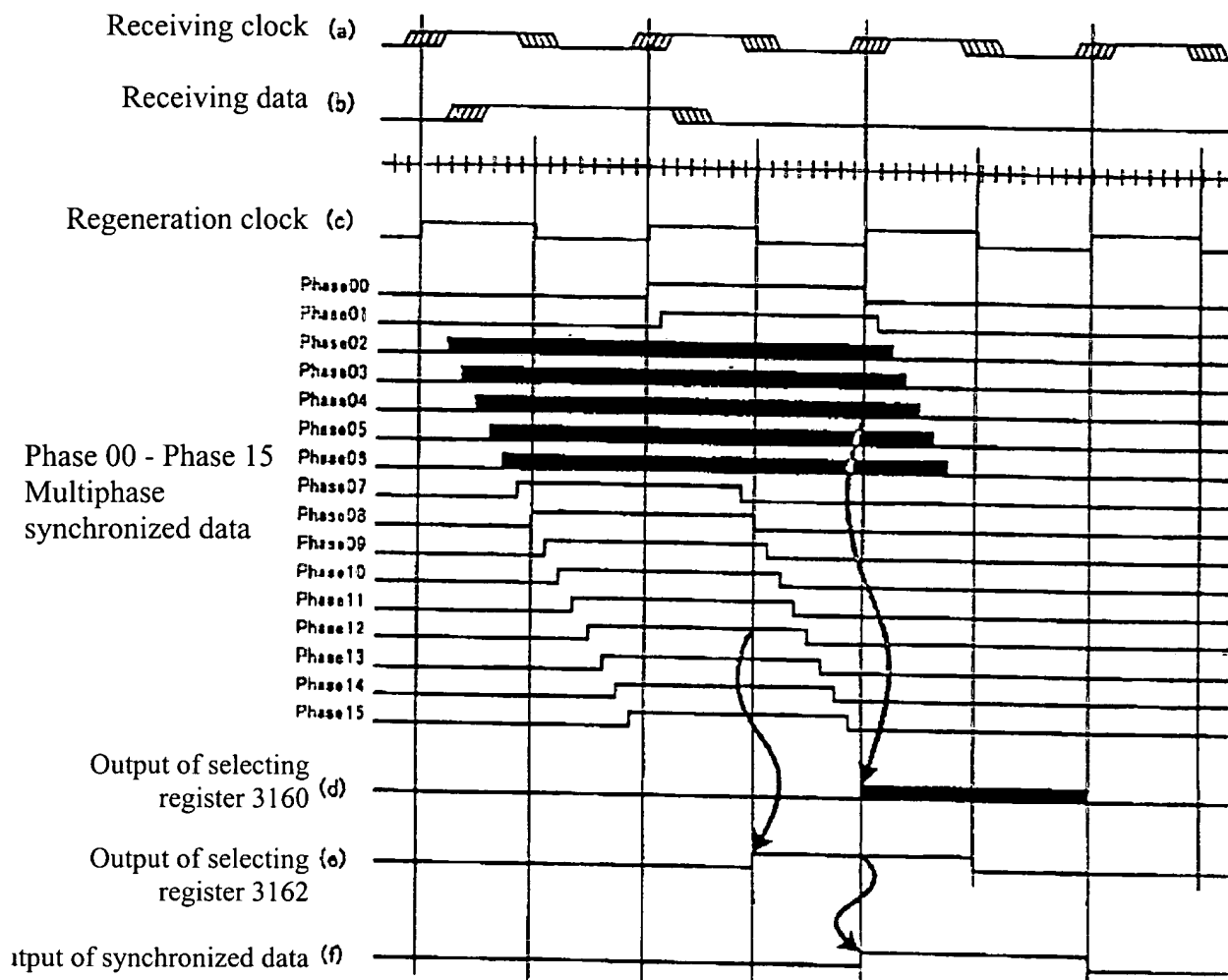


FIG. 17